AMENDMENTS

IN THE CLAIMS:

Please cancel claims 1-2, 8 and 14-17, and amend claims 3-4, 6 and 9 as provided below.

1-2. (Canceled).

3. (Currently amended) ~~The method of claim 1~~ A method for forming a ferroelectric capacitor comprising:

providing a dielectric layer over a semiconductor;

forming a barrier layer over said dielectric layer;

forming a first metal layer over said barrier layer;

forming a ferroelectric layer over said first metal layer;

forming a hard-mask layer over said second metal layer; and

etching said second metal layer, said ferroelectric layer, and said first metal layer using a three step plasma process comprising:

a first metal layer etch comprising the gases Cl2, O2, N2, and CO;

a PZT etch comprising the gases BCl3 and Cl2; and

a second metal layer etch comprising the gases Cl2, O2, N2, and CO,

wherein said plasma process comprises a PZT etch process comprising the gases BCl3 and Cl2 in a range of ratios from 1:4 to 10:1 respectively.

4. (Currently amended) The method of claim [[1]] 3, wherein said first metal layer comprises iridium, said ferroelectric layer comprises PZT, and said second metal layer comprises iridium.

5. (Original) The method of claim 4 wherein said second metal layer comprises iridium.

6. (Currently amended) A method for forming a ferroelectric memory cell comprising:

providing a dielectric layer over a semiconductor;

forming a barrier layer over said dielectric layer;

forming a first metal layer over aid barrier layer;

forming a ferroelectric layer over said first metal layer;

forming a second metal layer over said ferroelectric layer;

forming a hard-mask layer over said second metal layer;

etching said first metal layer with a plasma process comprising the gases Cl2, O2, N2, and CO; and

etching said ferroelectric layer with a plasma process comprising the gases BCl3 and Cl2, wherein said ferroelectric layer etch process further comprises the gases BCl3 and Cl2 in a range of ratios from 1:4 to 10:1 respectively.

7. (Original) The method of claim 6 wherein all etch process are performed at temperatures between 200°C and 500°C.

8. (Canceled).

9. (Currently amended) The method of claim [[8]] 6, wherein said first metal layer comprises iridium and said ferroelectric layer comprises PZT.

10. (Original) A method for forming a ferroelectric memory capacitor comprising:

providing a dielectric layer over a semiconductor wherein said dielectric layer has an upper surface forming a plane;

forming a barrier layer over said dielectric layer;

forming a first metal layer over said barrier layer;

forming a ferroelectric layer over said first metal layer;

forming a second metal layer over said ferroelectric layer;

forming a hard-mask layer over said second metal layer; and

etching said second metal layer, said ferroelectric layer, and said first metal layer using a plasma process to form sidewalls wherein the angle forming by said sidewalls and said plane is between 78°and 88°.

11. (Original) The method of claim 10 wherein said plasma process comprises a three step process, comprising:

a first metal layer etch comprising the gases Cl2, O2, N2, and CO;

a PZT each comprising the gases BCl2 and Cl2; and

a second metal layer etch comprising the gases Cl2, O2, N2, and CO.

12. (Original) The method of claim 10 wherein said plasma process comprises a PZT etch process comprising the gases BCl3 and Cl2 in a range of ratios from 1:4 to 10:1 respectively.

13. (Original) The method of claim 11 wherein said first metal layer comprises iridium, said ferroelectric layer comprises PZT, and said second metal layer comprises iridium.

14-17. (Canceled).